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Charles A Johnson
Unisys Corporation
Law Department M S 4773
2470 Highcrest Road
Roseville, MN 55113

EXAMINER

VITAL, PIERRE M

ART UNIT

PAPER NUMBER

2188

DATE MAILED: 12/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/651,597

Applicant(s)

ENGLIN ET AL.

Examiner

Pierre M. Vital

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 3, 2003 has been entered.

Response to Amendment

2. This Office Action is in response to applicant's communication filed December 3, 2003 in response to PTO Office Action mailed October 29, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

3. Claims 1-20 have been presented for examination in this application. In response to the last Office Action, claims 1, 2, 6, 10, 11, 16-20 have been amended. No claims have been canceled or added. As a result, claims 1-20 are now pending in this application.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claim recites the limitation "a level two cache memory which is directly coupled to a level three memory". As shown in Figs. 2 and 4, it appears that the voyager IP 50 which contains the level two cache is coupled to the third level cache 48 by means of the third level cache controller 26. Note that page 14, lines 6-8 of the specification discloses that the bus interface logic 60 of Fig. 4 couples the system controller 50 with the third level cache controller 26. Furthermore, Fig. 2 shows that controller 50 is directly coupled to the third level cache controller 26, but not to the third level cache 48. Applicant is requested to provide where support for this limitation can be found in the drawings and/or the specification or to amend the claim to rectify this discrepancy.

Claims 2-5 directly or indirectly dependent on claim 1 are rejected for the reasons stated above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

See 7. Claims 11 and ~~18~~¹⁶ rejected under 35 U.S.C. 102(b) as being anticipated by Kranich (US5,850,534).

As per claim 11, Kranich discloses a method of maintaining validity of data within a level one cache memory of a processor having a level one tag memory [*level one tag array 213 of level one cache 20; Fig. 2*] directly coupled to a level two cache memory containing a tag memory and a data memory [*level 1 cache 20 is directly coupled to level 2 cache 30; Fig. 1; level 2 tag array 203 of level 2 cache 30; Fig. 2*] wherein said level two cache memory is directly coupled to a system memory bus [*level 2 cache 30 is directly coupled to bus 40; Fig. 1*] comprising: formulating a SNOOP request [*monitoring is performed by a snooping process; col. 2, lines 6-7*]; presenting said SNOOP request on said system memory bus to said level two cache memory [*the level 2 cache snoops the external accesses over the shared memory bus; col. 2, lines 14-15*]; routing said SNOOP request directly to said tag memory [*the snoop process includes examines the tag array; col. 2, lines 6-10*]; processing said SNOOP request [*the snoops results in a level 2 cache hit; col. 2, lines 21-29*].

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- 8.4.4 As per claim ¹⁶18, Kranich discloses an apparatus comprising:
- a. means for executing program instructions [*processors 10-12; Fig. 1*];
 - b. means directly coupled to said executing means for level one caching data [*level 1 caches 20-22 are directly coupled to processors 10-12; Fig. 1*];
 - c. means directly coupled to said executing means and said level one caching means for requesting a data element if said executing means requires requesting of said data element and said level one caching means does not contain said data element [*level 1 cache controller 211; Fig. 2*];
 - d. means directly coupled to said requesting means for level two caching [*level 2 cache 30-32 directly coupled to level 1 caches 20-22 which contain controller 211; Fig. 1*];
 - e. means located within said level two caching means for storing level two caching data [*data array 205; Fig. 2*];
 - f. means located within said level two caching means for maintaining level two tags [*level 2 tag array 203 of level 2 cache 30; Fig. 2*];
 - g. means directly coupled to said maintaining means for directly snooping said level two tags [*highest level cache includes a means for monitoring the shared memory bus; col. 3, lines 43-44; monitoring is performed by a snooping process; col. 2, lines 6-7; the snoop process includes examines the tag array; col. 2, lines 6-10*].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1, 6, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094).

As per claims 1 and 6, Kranich discloses a data processing system including a plurality of processors each directly coupled via a system memory bus [*processors 10-12 coupled to each other by memory bus 40; Fig. 1*], wherein a first processor of said plurality of processors contains a level one cache memory directly coupled to a level two cache memory which is directly coupled to a level three memory [*level 2 cache is operatively coupled to level 1 cache and higher level caches are operatively coupled to next lower level cache; col. 3, lines 29-34; Fig. 1*]; said level two cache memory containing cache storage and tag storage [*level 2 cache 30 contains data array 205 and tag array 203; Fig. 3*], and containing a circuit for SNOOPing said system memory bus [*the highest level cache includes a means for monitoring the shared memory bus; col. 3, lines 43-44*].

However, Kranich does not specifically teach the improvement comprising a first dedicated path between said system bus and said cache storage and a second dedicated path between said system bus and said tag storage as recited in the claim.

Kumar discloses a data processing system for reducing cache latency wherein the improvement comprises a first dedicated path between a system bus and a cache

storage [front side bus 190 communicates with L2 data array by means of line connected to way predictor 150; Fig. 7], and a second dedicated path between a system bus and a tag storage [front side bus 190 communicates with L2 tag array 135 by means of snoop queue line; Fig. 7], in order for the microprocessor to directly access the cache tag array without accessing the external bus during a lookup [col. 5, lines 24-32].

Note that Kumar discloses that the combination of the cache tag array 55 and cache data array 60 in Fig. 3 could serve as a secondary cache as detailed in col. 6, lines 1-10.

Therefore, it would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Kumar before him at the time the invention was made, to modify the system of Kumar because a dedicated path is well known to benefit with reduced cache latency so that the microprocessor to directly access the cache tag array without accessing the external bus during a lookup.

As per claim 7, Kranich discloses a data request transferred from said level one cache memory to a level two cache memory [if level 1 cache does not have the requested address, the level 2 cache will next try to service the processor address request; col. 4, lines 41-43].

10. Claims 2, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765).

As per claims 2 and 8, the combination of Kranich and Kumar discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Kumar do not specifically teach a control logic which provides the highest priority for a SNOOPing as recited in the claims.

Stevens discloses a control logic which provides the highest priority for a SNOOPing [col. 4, lines 23-32], in order to provide minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Kumar and Stevens before him at the time the invention was made, to modify the system of Kranich and Kumar because a control logic which provides the highest priority for snooping benefits by providing minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency [col.4, lines 15-20] as taught by Stevens et al.

11. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765) and further in view of Duncan (US6,353,877).

As per claims 3, the combination of Kranich and Kumar and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Kumar and Stevens do not specifically teach do not specifically teach a level two cache comprising a duplicate tag memory as recited in the claim.

Duncan discloses a multiprocessing system comprising a duplicate tag store [col. 7, line 30], in order to facilitate a determination as to the contents of the other caches of the processor.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Kumar and Stevens and Duncan before him at the time the invention was made, to modify the system of Kranich and Kumar and Stevens because a duplicate tag store benefits by maintaining cache coherency by facilitating a determination as to the contents of the other caches of the processor [col. 7, lines 20-32] as taught by Duncan.

As per claim 4, Kranich discloses said plurality of processors further comprises a plurality of instruction processors [*processors make requests*; col. 4, lines 34-35].

As per claim 5, Kumar discloses said level three memory further comprises a level three cache memory [*third level cache, L2*; col. 9, line 24; Fig.7].

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765) and further in view of Fu (US6,457,087).

As per claim 9, Kranich discloses a data processing system comprising a level one tag memory located within a level one cache memory [*tag array 213 in level 1 cache memory*; Fig. 2].

However, the combination of Kranich and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Stevens do not specifically teach a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory.

Fu discloses a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within a level one tag memory [*i.e., L2 duplicate tag memory 234*] [Fig. 5A] in order to provide an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Fu before him at the time the invention was made, to modify the system of Kranich and Stevens to include a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory

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because it would have provided an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system [col. 31, lines 11-16] as taught by Fu.

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Kumar et al (US6,247,094) and Stevens et al. (US5,426,765) and Fu (US6,457,087) and further in view of Duncan (US6,353,877).

As per claim 10, the combination of Kranich and Kumar and Stevens and Fu discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Kumar and Stevens do not specifically teach routing said SNOOP request to a duplicate tag memory and processing said SNOOP request regarding said duplicate tag memory as recited in the claims.

Duncan discloses snoop request is responsively coupled to a duplicate tag memory [col. 8, lines 11-13]; routing said SNOOP request to a duplicate tag memory [col. 8, lines 11-15]; processing said SNOOP request regarding said duplicate tag memory [col. 8, lines 11-20] to determine if the requested block is present in the respective caches.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Kumar and Stevens and Fu and Duncan before him at the time the invention was made, to modify the system of Kranich and Kumar and Stevens

and Fu because coupling snoop request to a duplicate tag memory benefits in monitoring the bus by determine if the requested block is present in the respective caches [col. 8, lines 10-15] as taught by Duncan.

14. Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765).

As per claims 12 and 17, Kranich discloses a data request transferred from said level one cache memory to a level two cache memory [*if level 1 cache does not have the requested address, the level 2 cache will next try to service the processor address request*; col. 4, lines 41-43].

However, Kranich does not specifically teach a control logic which provides the highest priority for a SNOOPing as recited in the claims.

Stevens discloses a control logic which provides the highest priority for a SNOOPing [col. 4, lines 23-32], in order to provide minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens before him at the time the invention was made, to modify the system of Kranich because a control logic which provides the highest priority for snooping benefits by providing minimal effect on system speed by allowing the

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cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency [col.4, lines 15-20] as taught by Stevens.

15. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and further in view of Fu (US6,457,087).

As per claim 13, the combination of Kranich and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Stevens do not specifically teach a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory.

Fu discloses a data processing system comprising a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within a level one tag memory [*L2 duplicate tag memory 234*; Fig. 5A] in order to provide an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Fu before him at the time the invention was made, to modify the system of Kranich and Stevens to include a data processing system comprising a level two cache memory further comprising a duplicate tag

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memory which maintains a duplicate of information within said level one tag memory because it would have provided an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system [col. 31, lines 11-16] as taught by Fu.

16. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and Fu (US6,457,087) and further in view of Duncan (US6,353,877).

As per claims 14 and 15, the combination of Kranich and Stevens and Fu discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Stevens do not specifically teach routing said SNOOP request to a duplicate tag memory and processing said SNOOP request regarding said duplicate tag memory as recited in the claims.

Duncan discloses routing said SNOOP request to a duplicate tag memory [col. 8, lines 11-15]; processing said SNOOP request regarding said duplicate tag memory [col. 8, lines 11-20] to determine if the requested block is present in the respective caches.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Fu and Duncan before him at the time the invention was made, to modify the system of Kranich and Stevens and Fu because routing and processing snoop request to a duplicate tag memory benefits in monitoring

the bus by determine if the requested block is present in the respective caches [col. 8, lines 10-15] as taught by Duncan.

17. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and Kumar et al (US6,247,094).

As per claim 18, Kranich discloses means directly coupled to said level two caching means for bussing system memory data [shared memory bus 40; Fig. 1]; means directly coupled to said bussing means for interfacing said bussing means directly to said storing means [*level 2 cache is directly coupled to bus 40; Fig. 1*].

However, the combination of Kranich and Stevens does not specifically teach means directly coupled to said bussing means for interfacing said bussing means directly to said maintaining means as recited in the claim.

Kumar discloses a data processing system for reducing cache latency wherein means directly coupled to a bussing means for interfacing said bussing means directly to a maintaining means [*front side bus 190 communicates with L2 tag array 135 by means of snoop queue line; Fig. 7*], in order for the microprocessor to directly access the cache tag array without accessing the external bus during a lookup [col. 5, lines 24-32].

Note that Kumar discloses that the combination of the cache tag array 55 and cache data array 60 in Fig. 3 could serve as a secondary cache as detailed in col. 6, lines 1-10.

Therefore, it would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Kumar before him at the time the invention was made, to modify the system of Kumar because directly accessing a maintaining means benefits with reduced cache latency so that the microprocessor to directly access the cache tag array without accessing the external bus during a lookup.

18. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and Kumar et al (US6,247,094) and further in view of Fu (US6,457,087).

As per claim 13, the combination of Kranich and Stevens and Kumar discloses the claimed invention as detailed above in the previous paragraphs. Kranich further discloses means located within said level one caching means for recording level one tags [*level 1 tag array 213*; Fig. 2]. However, Kranich and Stevens and Kumar do not specifically teach means located within said level two caching means and directly coupled to said recording means for duplicating said level one tags as recited in the claim.

Fu discloses means located within a level two caching means and directly coupled to a recording means for duplicating level one tags [*L2 duplicate tag memory 234*; Fig. 5A] in order to provide an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Kumar and Fu before him at the time the invention was made, to modify the system of Kranich and Stevens and Kumar to include means located within a level two caching means and directly coupled to a recording means for duplicating level one tags because it would have provided an improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system [col. 31, lines 11-16] as taught by Fu.

19. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kranich (US5,850,534) and Stevens et al. (US5,426,765) and Kumar et al (US6,247,094) and Fu (US6,457,087) and further in view of Duncan (US6,353,877).

As per claim 20, the combination of Kranich and Stevens and Kumar and Fu discloses the claimed invention as detailed above in the previous paragraphs. However, Kranich and Stevens and Kumar and Fu do not specifically teach means directly coupled to said bussing means and said duplicating means for snooping said duplicating means as recited in the claim.

Duncan discloses means directly coupled to said bussing means and said duplicating means for snooping said duplicating means [col. 8, lines 11-20] to determine if the requested block is present in the respective caches.

It would have been obvious to one of ordinary skill in the art, having the teachings of Kranich and Stevens and Fu and Duncan before him at the time the invention was made, to modify the system of Kranich and Stevens and Fu because routing and processing snooping a duplicate means benefits in monitoring the bus by determine if the requested block is present in the respective caches [col. 8, lines 10-15] as taught by Duncan.

Response to Arguments

20. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach multilevel cache memory and prioritizing snoop request over processor request.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Puv

Pierre M. Vital
Art Unit 2188
December 12, 2003

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER